D-PHY Transmitter Test, Receiver, and Protocol Solutions

D-PHYTX, D-PHYXpress, SR-DPHY, and Moving Pixel Datasheet

Key features

Transmitter testing:
- Test time
  - Fully automated solution: Performs D-PHY transmitter test with single-button click, seamlessly across High Speed (HS), Low Power (LP), Low Power-High Speed (LP-HS) and Ultra-Low Power State (ULPS) sequences in the D-PHY signal.
  - Allows to select individual test or group-wise tests through the tree structure.
  - RF Switch support to handle multi-lane test with zero manual intervention.
- 100% test coverage as per D-PHY v1.2, CTS v1.2
  - Performs all fully-automated tests, including Bus Turn Around (BTA) and Ultra-Low Power State (ULPS) measurements, as per D-PHY specifications up to v1.2.

Debug features
- Modify limits of test parameters in TekExpress for debug and characterization.
- Provides DPOJET based setup files to debug the root cause analysis of failures.

Measurement accuracy
- D-PHYTX application handles multitude scenarios like Continuous or Burst mode, Termination variations, and varying idle time.

Transmitter conformance test and beyond
- Custom limits to perform margin testing
- Performs characterization by running TekExpress application in continuous mode and collect the data.

Signal access
- P7700 Series High Impedance TriMode probe designed especially for MIPI application, that requires low loading, single-ended/differential measurements.
- Provides TekFlex™ accessories for flexible probing

Offline/Remote analysis
- Analyze live or pre-acquired waveforms
- Allows remote execution of tests

1 See the host system requirements in the Ordering Information section.
Receiver testing:

- Simplified Receiver test setup
  - Single setup to generate signal for D-PHY and C-PHY
  - Easy to calibrate and provide repeatable result
  - Direct synthesis method helps to create all types of stress with a single box.

- Test Coverage
  100% Test coverage: D-PHYXpress application allows you to create D-PHY standard conformant test signals as per MIPI D-PHY v1.2 and v2.0 specifications.

- Signal Fidelity
  Best in class AWG70000 series with sampling rate of 50 GS/s with 10 bit vertical resolution, to provide best signal fidelity for D-PHY signal generation.

- Ease of Use
  D-PHYXpress provides batch processing to create multiple test scenarios for rigorous test requirements.

- Receiver conformance test and beyond
  - D-PHYXpress application provides a platform for you to create wide range of stimuli to test the device beyond specification.
  - You can program Data to Clock timing, Rise time and Fall time of Data/Clock, Program ESC, LP Command along with Programmable Stress as mentioned below:
    - HS mode stressors
    - Random Jitter and Deterministic Jitter
    - Embed Insertion Loss and De-emphasis
    - Spread Spectrum Clocking
    - Dynamic Skew (D-PHY)
    - LP mode stressors
    - $e_{Spike}$ and Minimum Pulse $T_{MIN-RX}$
    - Set up/hold time tolerance
    - Real-time skew control

- Offline signal generation
  D-PHYXpress application can work in offline mode or from PC to control AWG remotely and generate D-PHY signals.

Scope based DSI-1 and CSI-2 Protocol Decode:

- Decodes DSI and CSI-2 buses in Low Power and High Speed states.
- Decodes both short packets, long packets and communications types such as Bus Turn Around (BTA), Escape Mode Commands, and Low Power data.
- Decodes the DCS command, ECC, checksum, data type, packet data, and others.
- Displays event table, search, and error indicators.
- Indicates missing sync, ECC, and checksum errors.

Moving Pixel D-PHY Protocol Generator and Decoder:

- D-PHY Protocol Generator
  - Supports up to D-PHY v1.2, CSI v1.2, and DSI v1.2 protocols.
  - Standalone instrument with simplified setup and operation.
  - Supports MIPI D-PHY signaling up to 2.5 Gbps-per-lane, for 1-4 lanes.
  - Provides automated video sequence construction according to the user-defined frame timing.
  - Supports command insertion during looping video upon user command.
  - Provides extensive scripting and macro-capability (macros can now contain video mode frames).

- D-PHY Protocol Decoder
  - Monitors MIPI D-PHY traffic up to 2.5 Gbps-per-lane, for 1-4 lanes.
  - Standalone instrument with simple setup and operation.
  - Provides Sniff Mode (high-Z) and Receive Mode (SMA, terminated) interfaces.
  - Supports acquisition of contiguous D-PHY traffic using 1 GB capture memory.
  - Provides Protocol Packet triggering, LP sequencing and State triggering, and ECC/CRC/Burst Error triggering.
  - Provides real-time statistics: Bus activity, measured bit-rate, packet counts, and ECC/CRC error counts, etc.
  - Acquires, decodes, and displays CSI2 v1.2, DSI v1.2 protocol packets and D-PHY 1.2 signaling states (earlier standards are also supported).
  - Provides extensive search and display filtering capabilities.
  - Provides extensive RPC remote-control capability.

Applications

D-PHY testing for:

- Automotive camera and display
- Mobile camera and display
- D-PHY interface design
- DSI-1 or CSI-2 verification
- System validation and integration
- Manufacturing test
Transmitter testing

The Tektronix TekExpress® (TEKEXP) Automated Test software runs on Windows 7 operating system.

TekExpress software ordered with Option D-PHYTX provides an automated, simple, and efficient way to test D-PHY Transmitter interfaces and devices consistent to the requirements of the D-PHY Conformance Test Specification revision up to v1.2.

Automated testing – save time and resources

D-PHYTX allows you to select the desired tests to run and test the multiple lanes that to be tested. The automated solution, allows you to focus on design and debug of the measurements.

Setup test execution and reporting of measurements

Setup and test execution is simple with the TekExpress D-PHYTX software. The oscilloscope is controlled through the TekExpress automation framework. The TekExpress software provides a Graphical User Interface (GUI) and provides an intuitive workflow through setup and testing. D-PHYTX application provides GUI to select Test specification, Tree structure of HS, LP, HS-LP tests as per specifications, and Configuration for test condition.

Setting up the bench

You can view the schematic of the selected test with a push of a button. It also displays graphical representation of the test connection to avoid human errors.

Pass/fail report

The report tab provides a view of test results along with pass or fail status, test margin, and images supporting the test results for each lane of the DUT.

Beyond conformance - D-PHY Transmitter testing with D-PHY Essentials

DPOJET software with Option D-PHY provides the essential set of D-PHY Transmitter measurements with greater flexibility in the test setup. This option allows engineers to test device beyond conformance.

The following table outlines the key benefits from the DPOJET Option D-PHY and the TekExpress Option D-PHYTX software solution.

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<th>Feature</th>
<th>Option D-PHY (D-PHY Essentials)</th>
<th>Option D-PHYTX (D-PHYTX Automated Solution)</th>
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<td>Prerequisite tools</td>
<td>DPOJET Timing and Analysis</td>
<td>TEKEXP Automation</td>
</tr>
<tr>
<td>Automatic measurement selections based on device ID, test group, and selected probes</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>Single-button execution for all measurements</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>Configurable setup and editing of test limits</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Detailed or summary reports</td>
<td>Detailed only</td>
<td>Detailed and Summary</td>
</tr>
<tr>
<td>Automatically save test reports and waveforms</td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>Re-analyze prerecorded waveforms</td>
<td>✓</td>
<td>✓</td>
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<tr>
<td>D-PHY specific user interface</td>
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</tr>
<tr>
<td>Conformance test specification revision</td>
<td>up to v1.2</td>
<td>up to v1.2</td>
</tr>
</tbody>
</table>
P7700 probe for MIPI D-PHY

MIPI D-PHY application needs special type of probing as it operates in different impedance mode in High Speed and Low Power mode. In High Speed mode, D-PHY signals operate in terminated mode with differential signaling. In Low Power mode, D-PHY signal is operated in unterminated mode with single-ended signals. MIPI D-PHY has two main requirements for probing:

- Provide high impedance
- Differential and single-ended mode

P7700 series probe provides active buffer tip designed for Low Probe loading few millimeters from end of tip to provide best signal fidelity for MIPI D-PHY application along with flexible connectivity options.

With TriMode probing, probe setup makes differential, single-ended, and common mode measurements accurately. This unique capability allows you to work more effectively and efficiently, switching between differential, single-ended and common mode measurements without moving the probe’s connection points.

You can be confident in the signal fidelity of your measurements. The innovative new probe design uses SiGe Technology to provide the bandwidth and fidelity needed today and in the future.

The P7700 series probe architecture provides:

- An active buffer amplifier on the tips with the probe input only 3.2 mm from the input
- Excellent step response and low insertion loss up to 20 GHz
- Low-DUT loading with 100 kΩ (DC) and 0.4 pF (AC) performance
- High CMRR
- Low noise

Switch Matrix support

The D-PHY application supports Switch Matrix option which enables fully automated testing for multi-lane D-PHY Transmitter test.

Advantages of Switch Matrix for D-PHY application:

- Multilane Testing: Switch Matrix eliminates reconnection and reduces errors through automating test setup for each lane of a multilane D-PHY bus.
- De-embed loss of Switch using S-Parameters to perform accurate measurements.

Test coverage

D-PHYTX application provides 100% test coverage as per D-PHY v1.2. For more details, refer to the Transmitter test specification table.

Receiver testing

The D-PHYXpress plugin creates D-PHY signals for High Speed, High Speed Burst, and Low Power content with worst-case impaired input signals.

Receiver test solution follows the below steps:

- Generate test signal to emulate the transmitter including channel and noise impairments.
- Calibrate the signal as per the CTS requirement.
- Setup the Device for the receiver test.
- Determine the Bit Error Rate in the given test condition.

The D-PHYXpress application addresses the capabilities in the following step 1 and step 2:

**Step 1: Generate test signal to emulate the transmitter including channel and noise impairments**

The D-PHYXpress supports waveform generation for High Speed, Low Power, and Low Power-High Speed (LP-HS) mode as per D-PHY specification up to v2.0.
**High Speed mode:** The D-PHY v2.0 specification data rate is up to 4.5 Gbps in High Speed mode. As per CTS, you need to emulate the channel effect in High Speed mode. D-PHYXpress application allows you to edit the data rate, rise time, pattern type, voltage level, and impairments to emulate the channel effect.

**High Speed Jitter - Jitter**

In High Speed mode, you can add various channel effect such as: Periodic Jitter (Pj), Random Jitter (Rj), Dynamic Skew, Sine Noise Amplitude, Data to Clock Skew, De-Emphasis, S-Parameter file of Channel for Data and Clock, and SSC on Clock signal.

**High Speed Jitter - De-Emphasis**

**High Speed Jitter - Embed Channel**

**Low Power mode:** The D-PHY v2.0 specification data rate is up to 100 MHz in Low Power mode. The D-PHYXpress application allows you to edit data rate, rise time, pattern type, voltage level, and impairments to emulate the channel effect.

**Low Power**

The D-PHY v2.0 specification requires Sine/Square noise with eSpike noise.

**LP-HS mode:** The D-PHYXpress allows you to add Sync Word as per the specification with timing parameters for Data and Clock.
LP-HS mode

Step 2: Calibrate the signal as per CTS requirement

Calibration of signal impairments provides calibration routines that are D-PHY standard specific. The objective of calibration is to compensate the patterns for specific jitter parameters. The typical parameters are Random, Periodic Jitter, and Amplitude. The procedure sequences through all the patterns and each pattern is calibrated independently. These values are used for the Jitter controlled generation of patterns and are injected into the DUT during loopback.

Test coverage

For more details, refer to the Receiver test specification table.

Batch mode

Batch mode allows you to create a library of compiled waveforms with incremental Jitter value with a single click.

Scope-based decode for DSI-1 and CSI-2

The SR-DPHY application option enables decoding of DSI-1 and CSI-2 buses. SR-DPHY displays all the decoded components of short packets, long packets, and other communications types such as Bus Turn Around (BTA) and Escape Mode commands. In addition, DCS packets decode the DCS command.

Low-power states: High Speed (LPS HS), Escape (LPS escape), and Bus Turn Around (LPS BTS).

High Speed: Start-of-Transmission (SoT), Short Packets (SP), Long Packets (LgP), and End of Transmission (EoT).

Escape: Escape command (Low-Power data, Ultra-Low Power, Reset trigger, Tearing effect, and Acknowledge) and Low-Power data – will decode as packet data (SP/LgP).

Short packets: Data Type, Virtual Channel, Packet data byte 1, Packet data byte 2, and Error Correcting Code.
Long packets: Data Type, Virtual Channel Word Count, Payload (decoded as pixels or bytes depending upon data type), and Error correcting code.

In addition to decoding DSI-1/CSI-2 acquisitions, SR-DPHY also searches through long acquisitions to find all occurrences of the following packet types:

- Short Packets (specify VC, DT, direction, and packet data values)
- Long Packets (specify VC, DT, direction, WC, and data payload including pixel values)
- Start-of-Transmission (SoT), Stop, End-of-Transmission (EoT), Bus Turn Around (DSI-1 only), Escape mode, ECC warning, ECC error, and Checksum error.

### Moving pixel protocol solution


### Required equipment for D-PHY Transmitter and Receiver testing

For a complete list of required equipment, visit [http://www.tek.com/mipi-0](http://www.tek.com/mipi-0).
### Specifications

All specifications apply to all models unless noted otherwise.

#### Transmitter test specification

<table>
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<tr>
<th>D-PHY base specification</th>
<th>Revision 1.1 and 1.2</th>
</tr>
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<tbody>
<tr>
<td>D-PHY conformance specification</td>
<td>Revision 1.2</td>
</tr>
</tbody>
</table>

#### Measurements

- Both High Speed and Low Power modes, including ULPS and BTA.

#### Group 1 tests

**Data lane LP-TX signaling**

1. **1.1** Data lane LP-TX Thevenin output high level voltage (VOH)
2. **1.2** Data lane LP-TX Thevenin output low level voltage (VOL)
3. **1.3** Data lane rise time
4. **1.4** Data lane fall time
5. **1.5** Data lane LP-TX slew rate versus CLOAD (δV/δtSR)
6. **1.6** Data lane LP-TX pulse width of exclusive-OR clock (TLP-PULSE-TX)
7. **1.7** Data lane LP-TX period of exclusive-OR clock (TLP-PER-TX)

#### Group 2 tests

**Clock lane LP-TX signaling**

1. **1.2.1** Clock lane LP-TX Thevenin output high level voltage (VOH)
2. **1.2.2** Clock lane LP-TX Thevenin output low level voltage (VOL)
3. **1.2.3** Clock lane rise time
4. **1.2.4** Clock lane fall time
5. **1.2.5** Clock lane LP-TX slew rate vs. CLOAD (δV/δtSR)

#### Group 3 tests

**Data lane HS-TX signaling**

1. **1.3.1** Data lane HS entry: data lane TLPX value
2. **1.3.2** Data lane HS entry: THS-PREPARE value
3. **1.3.3** Data lane HS entry: THS-PREPARE + THS-ZERO value
4. **1.3.4** Data lane HS-TX differential voltages (VOD(0), VOD(1))
5. **1.3.5** Data lane HS-TX differential voltage mismatch (ΔVOD)
6. **1.3.6** Data lane HS-TX single ended output high voltages (VOHHS(DP),VOHHS(DN))
7. **1.3.7** Data lane HS-TX common-mode voltages (VCMTX(1),VCMTX(0))
8. **1.3.8** Data lane HS-TX common-mode voltage mismatch (ΔVCMTX(1,0))
9. **1.3.9** Data lane HS-TX dynamic common-level variations between 50-450 MHz (ΔVCMTX(LF))
10. **1.3.10** Data lane HS-TX dynamic common-level variations above 450 MHz (ΔVCMTX(HF))
11. **1.3.11** Data lane HS-TX 20%-80% rise time (tR)
12. **1.3.12** Data lane HS-TX 80%-20% fall time (tR)
13. **1.3.13** Data lane HS exit: THS-TRAIL value
14. **1.3.14** Data lane HS exit: 30%-80% Post-EoT rise time (TREOT) value
15. **1.3.15** Data lane HS exit: TEO value
16. **1.3.16** Data lane HS exit: THS-EXIT value

#### Group 4 tests

**Clock lane HS-TX signaling**

1. **1.4.1** Clock lane HS entry: TLPX value
2. **1.4.2** Clock lane HS entry: TCLK-PREPARE value
## Transmitter test specification

<table>
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<th>Description</th>
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<tbody>
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<td>Clock lane HS entry: TCLK-PREPARE + TZERO value</td>
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<tr>
<td>1.4.4</td>
<td>Clock lane HS-TX differential voltages (VOD(0), VOD(1))</td>
</tr>
<tr>
<td>1.4.5</td>
<td>Clock lane HS-TX differential voltage mismatch (ΔVOD)</td>
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<tr>
<td>1.4.6</td>
<td>Clock lane HS-TX single ended output high voltages (VOHHS(DP), VOHHS(DN))</td>
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<tr>
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<td>Clock lane HS-TX 20%-80% rise time (tR)</td>
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<td>1.4.12</td>
<td>Clock lane HS-TX 80%-20% fall time (tF)</td>
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<tr>
<td>1.4.13</td>
<td>Clock lane HS exit: TCLK-TRAIL value</td>
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<td>1.4.14</td>
<td>Clock lane HS exit: 30%-80% Post-EoT rise time (TREOT) value</td>
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<td>1.4.15</td>
<td>Clock lane HS exit: TEOT value</td>
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<td>1.4.16</td>
<td>Clock lane HS exit: THS-EXIT value</td>
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<td>1.4.17</td>
<td>Clock lane HS clock instantaneous (UIINST)</td>
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<td>1.4.18</td>
<td>Clock lane HS Clock Delta UI (ΔUI)</td>
</tr>
</tbody>
</table>

### Group 5 tests

**HS-TX Clock-to-Data lane timing**

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<th>Section</th>
<th>Description</th>
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<tbody>
<tr>
<td>1.5.1</td>
<td>HS entry TCLK-PREV value</td>
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<td>1.5.2</td>
<td>HS exit TCLK-POST value</td>
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<tr>
<td>1.5.3</td>
<td>HS clock rising edge alignment to first payload bit</td>
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<tr>
<td>1.5.4</td>
<td>Data-to-Clock skew (TSKEW (TX))</td>
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<tr>
<td>1.5.5</td>
<td>Initial HS Skew Calibration Burst (TSKEWCAL-SYNC, TSKEWCAL)</td>
</tr>
<tr>
<td>1.5.6</td>
<td>Periodic HS Skew Calibration Burst (TSKEWCAL-SYNC, TSKEWCAL)</td>
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</tbody>
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### Group 6 tests

**LP-TX INIT, ULPS and BTA requirements**

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<th>Description</th>
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<td>INIT: LP-TX initialization period (TINIT,MASTER)</td>
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<td>1.6.2</td>
<td>ULPS entry: verification of clock lane LP-TX ULPS support</td>
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<tr>
<td>1.6.3</td>
<td>ULPS exit: transmitted TWAKEUP interval</td>
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<td>1.6.4</td>
<td>BTA: TX-Side TTA-GO interval value</td>
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<tr>
<td>1.6.5</td>
<td>BTA: RX-Side TTA-SURE interval value</td>
</tr>
<tr>
<td>1.6.6</td>
<td>BTA: RX-Side TTA-GET interval value</td>
</tr>
</tbody>
</table>

### Probing configuration

- Single-ended and differential acquisition

### Triggering

- Edge trigger for clock lane tests in clock continuous mode. Choice of width trigger and transition trigger for all other tests and all other modes

### Reports

- Excel xls, HTML, and MHT formats with zoom-in screen shots of the testing regions for each test
Datasheet

Receiver test specification

<table>
<thead>
<tr>
<th>D-PHY base specification</th>
<th>Revision 1.2 and 2.0</th>
</tr>
</thead>
<tbody>
<tr>
<td>D-PHY conformance specification</td>
<td>Revision 1.2 and 2.0</td>
</tr>
</tbody>
</table>

Group 1 tests  
**LP-RX voltage and timing requirement**
- 2.1.1 LP-RX Logic 1 Input Voltage (VIH)
- 2.1.2 LP-RX Logic 0 Input Voltage, Non-ULP State (VIL)
- 2.1.4 LP-RX Input Hysteresis (VHYST)
- 2.1.5 LP-RX Minimum Pulse Width Response (TMIN-RX)
- 2.1.6 LP-RX Input Pulse Rejection (eSPIKE)
- 2.1.7 LP-RX Interference Tolerance (VINT and fINT)

Group 2 tests  
**LP-RX behavioral requirements**
- 2.2.1 LP-RX Initialization period (TINIT)
- 2.2.2 ULPS Exit: LP-RX TWAKEUP Timer Value
- 2.2.3 Clock Lane LP-RX Invalid/Aborted ULPS Entry
- 2.2.4 Data Lane LP-RX Invalid/Aborted Escape Mode Entry
- 2.2.5 Data Lane LP-RX Invalid/Aborted Escape Mode Command
- 2.2.7 Data Lane LP-RX Escape Mode, Ignoring of Post-Trigger-Command Extra Bits
- 2.2.8 Data Lane LP-RX Escape Mode Unsupported/Unassigned Commands

Group 3 tests  
**HS-RX voltage and set up/hold requirements**
- 2.3.1 HS-RX Common Mode Voltage Tolerance (VCMRX(DC))
- 2.3.2 HS-RX Differential Input High Threshold (VIDTH)
- 2.3.3 HS-RX Differential Input Low Threshold (VIDTL)
- 2.3.4 HS-RX Single-Ended Input High Voltage (VIHHS)
- 2.3.5 HS-RX Single-Ended Input Low Voltage (VILHS)
- 2.3.6 HS-RX Common-Mode Interference 50MHz - 450MHz (ΔVCMRX(LF))
- 2.3.7 HS-RX Common-Mode Interference Beyond 450MHz (ΔVCMRX(HF))
- 2.3.8 HS-RX Setup/Hold and Jitter Tolerance
- 2.3.9 HS-RX Setup/Hold and Jitter Tolerance (Spec 2.0, Data rate >=2.5Gbps)

Group 4 tests  
**HS-RX timer requirements**
- 2.4.1 Data Lane HS-RX TD-TERM-EN Value
- 2.4.2 Data Lane HS-RX THS-PREPARE + THS-ZERO Tolerance
- 2.4.3 Data Lane HS-RX THS-SETTLE Value
- 2.4.4 Data Lane HS-RX THS-TRAIL Tolerance
- 2.4.5 Data Lane HS-RX THS-SKIP Value
- 2.4.6 Clock Lane HS-RX TCLK-TERM-EN Value
- 2.4.7 Clock Lane HS-RX TCLK-PREPARE + TCLK-ZERO Tolerance
- 2.4.8 Clock Lane HS-RX TCLK-SETTLE Value
- 2.4.9 Clock Lane HS-RX TCLK-TRAIL Tolerance
- 2.4.11 Clock Lane HS-RX TCLK-PRE and TCLK-POST Tolerance

Measurements  
Both High Speed and Low Power modes, including ULPS and BTA.

Refer to MOI for detailed procedure.
## Receiver test specification

### D-PHY specification coverage

<table>
<thead>
<tr>
<th>Standard</th>
<th>Specs version</th>
<th>Applicable SW options</th>
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<td>D-PHYTX</td>
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<td>D-PHY Receiver</td>
<td>up to v2.0</td>
<td>D-PHYXpress</td>
</tr>
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</table>
## Ordering Information

### D-PHYTX Automated

<table>
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<tr>
<th>Model</th>
<th>Description</th>
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</thead>
<tbody>
<tr>
<td>DPO7254/C</td>
<td>DPO (Digital Phosphor Oscilloscope), MSO (Mixed Signal Oscilloscope) Oscilloscopes - 3.5 GHz and above is recommended Where rise time accuracies are not a concern, a 2.5 GHz oscilloscope can also be used.</td>
</tr>
<tr>
<td>DPO7354/C</td>
<td></td>
</tr>
<tr>
<td>MSO70000/C</td>
<td></td>
</tr>
<tr>
<td>DPO70000B/C/DX/SX</td>
<td></td>
</tr>
<tr>
<td>TEKEXP</td>
<td>TekExpress® Automated Compliance Test Software</td>
</tr>
<tr>
<td>TEKEXP Opt. D-PHYTX</td>
<td>D-PHY Automated Solution for D-PHY Transmitter conformance, characterization, and verification <strong>Includes:</strong> Latest TekExpress product software DVD kit (P/N 020-2913-xx) and upgrade SW key. Online documentation and printable manual in PDF format are supplied.</td>
</tr>
<tr>
<td>TEKEXPUP Opt. D-PHYTX</td>
<td>D-PHY Automated Solution for D-PHY Transmitter conformance, characterization, and verification Order this option if TekExpress (TEKEXP) is already owned. The USB key dongle will be upgraded with Opt. D-PHYTX. <strong>Includes:</strong> Latest TekExpress product software DVD kit (P/N 020-2913-xx) and upgrade SW key. Online documentation and printable manual in PDF format are supplied.</td>
</tr>
</tbody>
</table>

### D-PHY Essentials

<table>
<thead>
<tr>
<th>Model</th>
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<tr>
<td>DPO7254/C</td>
<td>DPO (Digital Phosphor Oscilloscope), MSO (Mixed Signal Oscilloscope) Oscilloscopes - 3.5 GHz and above is recommended Where rise time accuracies are not a concern, a 2.5 GHz oscilloscope can also be used.</td>
</tr>
<tr>
<td>DPO7354/C</td>
<td></td>
</tr>
<tr>
<td>MSO70000/C</td>
<td></td>
</tr>
<tr>
<td>DPO70000B/C/DX/SX</td>
<td></td>
</tr>
<tr>
<td>DPOFL-D-PHY ²</td>
<td>D-PHY Essentials for D-PHY Transmitter testing Upgrade (floating license version)</td>
</tr>
<tr>
<td>Termination board</td>
<td>1 x TMPC-CTB D-PHY Termination board</td>
</tr>
</tbody>
</table>

² Requires DPOJET Jitter and Eye Analysis Tools (Opt. DJA).
SR-DPHY Decode

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSO/DPO5000</td>
<td>MIPI® D-PHY Serial Analysis DSI-1 and CSI-2</td>
</tr>
<tr>
<td>DPO70000C</td>
<td></td>
</tr>
<tr>
<td>MSO70000C</td>
<td></td>
</tr>
<tr>
<td>DPO70000C/D/SX</td>
<td></td>
</tr>
<tr>
<td>Opt. SR-DPHY</td>
<td></td>
</tr>
<tr>
<td>DPO-UP</td>
<td>MIPI® D-PHY Serial Analysis DSI-1 and CSI-2 upgrade</td>
</tr>
<tr>
<td>Opt. SR-DPHY</td>
<td></td>
</tr>
<tr>
<td>DPOFL-SR-DPHY</td>
<td>MIPI® D-PHY Serial Analysis DSI-1 and CSI-2 (floating license version)</td>
</tr>
</tbody>
</table>

Recommended probes for D-PHY Essentials or D-PHYTX Automated Solution

<table>
<thead>
<tr>
<th>Oscilloscope</th>
<th>Probes</th>
</tr>
</thead>
<tbody>
<tr>
<td>DPO70000/C</td>
<td>4x TAP2500/TAP3500/P6245</td>
</tr>
<tr>
<td></td>
<td>or 3x TDP3500 (Continuous clock)</td>
</tr>
<tr>
<td></td>
<td>or 4x TDP3500 (Non-continuous clock)</td>
</tr>
<tr>
<td>MSO70000/C</td>
<td>4x P7240</td>
</tr>
<tr>
<td>DPO70000B/C/SX</td>
<td>or 3x PT330/ PT340A/ PT360A/ PT380A/ PT313 (Continuous clock)</td>
</tr>
<tr>
<td></td>
<td>or 4x PT330/ PT340A/ PT360A/ PT380A/ PT313 (Non-continuous clock)</td>
</tr>
<tr>
<td></td>
<td>or 4x PT7700 series</td>
</tr>
</tbody>
</table>

D-PHY receiver setup

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>AWG70002A</td>
<td>10 bit, 2 G Samples record length, 2-channel arbitrary waveform generator</td>
</tr>
<tr>
<td>Options: 01/03/225</td>
<td></td>
</tr>
<tr>
<td>Option PRECOMFL-SS01 or PRECOMNL-SS01 on AWG</td>
<td></td>
</tr>
<tr>
<td>AWGSYNC01DPO-UP</td>
<td>Hub for synchronizing multiple AWGs</td>
</tr>
<tr>
<td>TMPC-MDC4500-4B</td>
<td>MIPI signal conditioning accessory for the AWG 70000</td>
</tr>
<tr>
<td>DPO70000C with opt DJA and Probe (For calibration purpose)</td>
<td>6-8 GHz real-time scope, required for Calibration</td>
</tr>
<tr>
<td>DPHYNL-SSV1</td>
<td>D-PHY synthesis software on AWG</td>
</tr>
<tr>
<td>PSPL 5915 with Opt.100PS</td>
<td>100 ps Filter (SMA male-to SMA male)</td>
</tr>
<tr>
<td>174-6606-00</td>
<td>SMA cables</td>
</tr>
<tr>
<td>174-5771-xx</td>
<td>Phase-matched SMA cable</td>
</tr>
</tbody>
</table>

3 Requires Microsoft Windows 7 OS.

4 Requires TPA-BNC TekProbe2 to TekVPI adapter.
Prerequisite host system software requirements for D-PHYTX Automated Solution for D-PHY Transmitter Conformance, Characterization, and Verification

Includes: Latest TekExpress product software DVD kit (P/N 020-2913-xx) and upgrade SW key. Online documentation and printable manual in PDF format are supplied D-PHYTX Automated Solution for D-PHY Transmitter Conformance, Characterization, and Verification. Order this option if TekExpress (TEKEXP) is already owned. The USB key dongle will be upgraded with Opt. D-PHYTX

Includes: Latest TekExpress product software DVD kit (P/N 020-2913-xx) and upgrade SW key. Online documentation and printable manual in PDF format are D-PHYTX

- Microsoft XP OS with SP2 or later, or Windows 7
- Microsoft Excel 2002 or above
- Microsoft Explorer 6.0 SP1 or later
- Adobe Reader 6.0 or equivalent software for viewing portable document format (PDF) files

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