DDR Analysis is a standard specific solution tool for Tektronix Performance Digital Oscilloscopes (DPO7000C or DSA/DPO/MSO70000C/D/DX series). DDR Analysis requires Jitter and Eye Diagram Analysis Tool (Option DJA) and the advanced Search and Mark capability (Option ASM). The DDRA/DDR-LP4 application includes compliance measurements and enables you to achieve new levels of productivity, efficiency, and measurement reliability.

Key features

- Memory Validation and Debug: Comprehensive support for validation of multiple memory standards including DDR4 and LPDDR4
- Selectable Speed Grades: Support for JEDEC defined speed grades as well as custom speeds
- Auto Configuration Wizard: Easily set up the test configuration for performing electrical validation
- Qualified Multi-Rank Measurements: Measurements can be done on a selected rank of interest
- Visual Trigger Integration in DDRA/DDR-LP4: Quickly setup a Visual Trigger definition for an event of interest and use this definition to gate the measurements performed by DDRA/DDR-LP4
- Cycle Type Identification: Navigate and timestamp all acquired read and write cycles
- Read & Write Burst Trigger Events: Quickly and easily isolate DQ, DQS and Clock signals using graphical based trigger systems
- De-embedding: Quickly select and apply De-embedding filters from within DDRA/DDR-LP4 to de-embed interposer and probe effects to accurately represent the signal
- Flexible Test Selection: Select the Memory specification and the Speed Grade for targeted analysis

Applications

Validating the memory interface at the physical layer for signal integrity as well as timing to achieve the desired level of power / performance goals as well as for interoperability.

Option DDRA on the DSO/MSO5000, DPO7000 and DPO/MSO70000 series of Oscilloscopes provides support for multiple memory standards at JEDEC defined speed grades as well as custom speeds. The following Memory standards are supported by DDRA/DDR-LP4:

- DDR, DDR2, DDR3, DDR3L, DDR4
- LPDDR, LPDDR2, LPDDR3, LPDDR4
- GDDR3, GDDR5
DDRA/DDR-LP4 configuration wizard

The configuration wizard in DDRA/DDR-LP4 provides a simple, step-by-step and easy to use interface to speed up the test process. The user selects the memory technology of interest, speed grade, measurement group (Reads, Writes, Clocks, Address and Control Lines) and individual measurements within the group from the DDRA/DDR-LP4 user interface.

De-embed filters

Easily de-embed the Interposer and the Probe effects by applying suitable de-embed filters from within DDRA/DDR-LP4. DDRA/DDR-LP4 also provides an option to apply custom filters.

Comprehensive measurements

Option DDR adds a long list of JEDEC specific measurements for different memory standards to the already existing rich tool set of generic jitter, timing and signal quality measurements in DPOJET.

<table>
<thead>
<tr>
<th>Memory type</th>
<th>JEDEC specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDR</td>
<td>JESD79E</td>
</tr>
<tr>
<td>DDR2</td>
<td>JESD79-2F</td>
</tr>
<tr>
<td>DDR3</td>
<td>JESD79-3F</td>
</tr>
<tr>
<td>DDR3L</td>
<td>JESD79-3-1</td>
</tr>
<tr>
<td>DDR4</td>
<td>JESD79-4A</td>
</tr>
<tr>
<td>LPDDR</td>
<td>JESD209B</td>
</tr>
<tr>
<td>LPDDR2</td>
<td>JESD209-2E</td>
</tr>
<tr>
<td>LPDDR3</td>
<td>JESD209-3B</td>
</tr>
<tr>
<td>LPDDR4</td>
<td>JESD209-4</td>
</tr>
<tr>
<td>GDDR5</td>
<td>JESD212</td>
</tr>
</tbody>
</table>

Burst detection

DDRA/DDR-LP4 provides different ways to detect bus cycles that will be used to make measurements:

- Built-in algorithms identify Read/Write cycles based on the DQ/DQS phase difference
- Qualify this with Chip Select for analysis targeted at specific Ranks
- MSO digital channel based Command Identification for Read/Write detection
- Defining Visual Trigger Areas to identify and gate area of interest for measurement
Results and reporting

Measurement configurations and JEDEC pass/fail limits are automatically applied for the selected measurements based on the memory specification and the speed grade selected. The results are included in statistics and plots to provide a complete analysis of the acquired waveform.

Hyperlinks within the report allow easy navigation between different sections in order to co-relate different measurement results.

Verification versus debug

DDRA/DDR-LP4 provides a comprehensive set of JEDEC measurements for different memory standards. In addition to this, it also provides access to the DPOJET advanced Jitter and Timing analysis engine that allows flexibility to reconfigure the existing measurements or to perform new measurements not defined by the JEDEC specification using new user specified test limits.

Also, features like logging, filters, histograms and time trends are available in DPOJET. This allows switching seamlessly between debug mode and verification mode.

Oscilloscope triggering and waveform identification

Tektronix Pinpoint® trigger system provides the most comprehensive high performance trigger system in the Industry. The Pinpoint trigger system encompasses threshold and timing related triggers, Dual A- and B-Event Triggering, Logic Qualification, Window Triggering, and Reset Triggering.
The Advanced Search and Mark feature on the Tektronix MSO/DPO5000, DPO7000, and MSO/DPO70000 Series Oscilloscopes finds unique events in waveforms. It scans acquired waveform data for multiple occurrences of an event and marks each occurrence. Search and Mark features have a close relationship with the Pinpoint trigger system since they both can be used to discriminate signal characteristics. Search and Mark includes signal-shape discrimination features of the Pinpoint trigger system and extends them across live channels, stored data and math waveforms.

**Pinpoint triggering**

Visual Trigger makes the identification of the desired waveform events quick and easy by scanning through all acquired analog waveforms and graphically comparing them to geometric shapes on the display. By discarding acquired waveforms which do not meet the graphical definition, Visual Triggering extends the oscilloscope’s trigger capabilities beyond the traditional hardware trigger system.

**Graphical triggering using Visual Trigger**

Visual Triggering extends the oscilloscope’s trigger capabilities beyond the traditional hardware trigger system.

**MSO70000 Series Oscilloscope probing command signals**

In order to perform analysis on the memory bus, access to the signal plays a very important role. JEDEC specification requires that the signals be probed at the balls of the memory device which are difficult to access.

To overcome this problem Tektronix, in partnership with Nexus Technology, is offering a variety of probing options such as BGA interposers that support different memory devices in a variety of form factors. The interposers include an embedded tip resistor placed very close to the BGA pad.

**Probing**

These capabilities of the oscilloscope are very useful during the debug and are also extensively used by DDRA/DDR-LP4 during the analysis.
Introduction of an interposer and the oscilloscope probe may change the characteristics of the signal. De-embedding filters can be used to remove the effect of the interposer and the probe in the signal path to get an accurate representation of the signal at the probe point.

<table>
<thead>
<tr>
<th>Technology</th>
<th>Package / form factor</th>
</tr>
</thead>
</table>
| DDR2       | Socketed – 60 Ball / 84 Ball  
Solder-down – 60 Ball / 84 Ball |
| DDR3       | Socketed – 78 Ball / 96 Ball  
Solder-down – 78 Ball / 96 Ball  
Edge Probe – 78 Ball / 96 Ball  
DIMM Interposer for MSO  
SO-DIMM Interposer for MSO |
| DDR4       | Socketed – 78 Ball / 96 Ball  
Edge Probe – 78 Ball / 96 Ball  
Edge Probe – 144 Ball  
DIMM Interposer for MSO |
| LPDDR      | Socketed – 60 Ball |
| LPDDR2     | Socketed – 136 Ball / 168 Ball / 216 Ball / 240 Ball |
| LPDDR3     | Socketed – 216 Ball  
Solder-down – 178 Ball |
| LPDDR4     | Socketed – 272 Ball  
Edge Probe – 272 Ball |
| GDDR5      | Socketed – 170 Ball  
Solder-down – 170 Ball |
### Logic debug and protocol analysis

When full protocol analysis or probing of the entire memory bus is required, a logic analyzer can provide this capability. The TLA7000 Series logic analyzers can also be linked with Tektronix oscilloscopes to provide an integrated test setup using tools such as iCapture mentioned above.

This eliminates the need for double probing and allows full analog capture of any signals probed by the logic analyzer. In addition, the iView™ display interface allows transfer of the oscilloscope data to the logic analyzer display, so that data from both instruments are analyzed and time-aligned on one display screen. Various types of probing solutions are available to support different form factors.

### Oscilloscope bandwidth considerations for memory analysis

#### (Category) specifications

<table>
<thead>
<tr>
<th>Memory technology</th>
<th>DDR</th>
<th>DDR2</th>
<th>DDR2</th>
<th>DDR3</th>
<th>DDR3</th>
<th>DDR3L</th>
<th>LPDDR3</th>
<th>LPDDR4</th>
<th>DDR4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Speed</td>
<td>all rates</td>
<td>to 400MT/s</td>
<td>to 800MT/s</td>
<td>to 1600MT/s</td>
<td>to 2400MT/s</td>
<td>to 1600MT/s</td>
<td>to 1600MT/s</td>
<td>to 4266MT/s</td>
<td>to 3200MT/s</td>
</tr>
<tr>
<td>Max slew rate</td>
<td>5</td>
<td>5</td>
<td>5</td>
<td>10</td>
<td>12</td>
<td>12</td>
<td>8</td>
<td>18</td>
<td>18</td>
</tr>
<tr>
<td>Typical V swing</td>
<td>1.8</td>
<td>1.25</td>
<td>1.25</td>
<td>1</td>
<td>1</td>
<td>0.9</td>
<td>0.6</td>
<td>0.3</td>
<td>0.8</td>
</tr>
<tr>
<td>20-80 risetime (ps)</td>
<td>216</td>
<td>150</td>
<td>150</td>
<td>60</td>
<td>50</td>
<td>45</td>
<td>45</td>
<td>27</td>
<td>27</td>
</tr>
<tr>
<td>Equivalent Edge BW</td>
<td>1.9</td>
<td>2.7</td>
<td>2.7</td>
<td>6.7</td>
<td>8.0</td>
<td>8.9</td>
<td>8.9</td>
<td>15.0</td>
<td>15.0</td>
</tr>
<tr>
<td>Recommended Scope BW (max performance)</td>
<td>2.5</td>
<td>3.5</td>
<td>4.0</td>
<td>12.5</td>
<td>12.5</td>
<td>12.5</td>
<td>12.5</td>
<td>16</td>
<td>16</td>
</tr>
</tbody>
</table>

1. Recommended scope BW (typical performance) 2

#### Notes

1. Highest accuracy on faster slew rates.

2. Slew rates are about 80% of the max specification. DDR3L, DDR4 and LPDDR3 is supported only on MSO/DPO70000C/D models only.
Ordering information

Models

DDRA
DDR Memory Bus Electrical Validation and Analysis Oscilloscope Software

DDR-LP4
LPDDR4 Memory Bus Electrical Validation and Analysis Oscilloscope Software

To order on a new DPO/MSO5000, DPO7000, DPO/MSO70000 Series:

Option DDRA
Preinstall on a new DPO5000, MSO5000, DPO7000, DPO70000, or MSO70000 Series oscilloscope

DPOFL-DDRA
DDR Memory Bus Electrical Validation and Analysis Oscilloscope Software – Floating License

Option DDR-LP4
Preinstall on a new DPO70000 or MSO70000 Series oscilloscope

DPOFL-DDR-LP4
LPDDR4 Memory Bus Electrical Validation and Analysis Oscilloscope Software – Floating License

To order on existing DPO/MSO5000, DPO7000, DPO/MSO70000 Series:

DPO-UP DDRA
Upgrade to Option DDRA (requires Options ASM and DJA)

DPO-UP DDR-LP4
Upgrade to Option DDR-LP4 (requires Option ASM, DJA and DDRA)

DPO-UP DJAE
Upgrade MSO/DPO5000 Series with DPOJET Jitter and Eye Diagram Analysis (Option DJA)

DPO-UP DJAM
Upgrade DPO7000 with DPOJET Jitter and Eye Diagram Analysis (Option DJA)

DPO-UP DJAH
Upgrade DPO70404 or DPO70804 or MSO70404 or MSO70804 with DPOJET Jitter and Eye Diagram Analysis (Option DJA)

DPO-UP DJAU
Upgrade DPO71254 or DPO73304 or MSO71254 or MSO72004 with DPOJET Jitter and Eye Diagram Analysis (Option DJA)

DPO-UP DJUP
DJA DPOJET software for oscilloscopes with both TDSJIT3 and TDSRTE licenses

To order floating licenses on existing DPO/MSO5000, DPO7000, DPO/MSO70000 Series:

DPOFL-DDRA
DDRA Package – Floating License

DPOFL-DDR-LP4
LPDDR4 Memory Bus Electrical Validation and Analysis Oscilloscope Software – Floating License

DPOFL-DJA
DPOJET Jitter and Eye Diagram Analysis – Floating License

3 DDR-LP4 is not available on DPO/MSO5000 and 7000 Series oscilloscopes.

4 DDR3L, DDR4, LPDDR3 and LPDDR4 are supported only on MSO/DPO70000C/D models.
### Recommended accessories

<table>
<thead>
<tr>
<th>Series</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>P7500</td>
<td>TriMode™ Differential Probe</td>
</tr>
<tr>
<td>020-2955-xx</td>
<td>Micro-coax Tips (TriMode) for P7500 Series Probes</td>
</tr>
<tr>
<td>020-3022-xx</td>
<td>Micro-coax Tips (TriMode) for P7500 Series Probes</td>
</tr>
<tr>
<td>020-2954-xx</td>
<td>Socket Cable for P7500 Series Probes</td>
</tr>
<tr>
<td>020-3131-xx</td>
<td>Long Reach Solder Tip with 75 Ω tip resistor for P7500 Series Probes</td>
</tr>
<tr>
<td>020-3135-xx</td>
<td>Long Reach Solder Tip with 0 Ω tip resistor for P7500 Series Probes</td>
</tr>
<tr>
<td>P7300</td>
<td>Z-Active™ Differential Probe (P7313, P7340A, P7360A, or P7380A)</td>
</tr>
<tr>
<td>020-2600-xx</td>
<td>Short Flex, Small Resistor Tip-Clip Assembly for P7300 Series Probes</td>
</tr>
<tr>
<td>020-2602-xx</td>
<td>Medium Flex, Small Resistor Tip-Clip Assembly for P7300 Series Probes</td>
</tr>
<tr>
<td>020-2604-xx</td>
<td>Long Flex, Small Resistor Tip-Clip Assembly for P7300 Series Probes</td>
</tr>
<tr>
<td>006-3415-xx</td>
<td>Antistatic Wrist Strap for P7300 Series Probes</td>
</tr>
<tr>
<td>P6780</td>
<td>Differential Logic Probe for MSO70000 Series Oscilloscopes</td>
</tr>
<tr>
<td>TDP3500</td>
<td>Differential Probe for MSO/DPO5000 and DPO7000 Series Oscilloscopes</td>
</tr>
</tbody>
</table>

### BGA interposers – by memory standard

<table>
<thead>
<tr>
<th>Memory</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDR2</td>
<td>x4, x8, x16 socketed and solder down interposers</td>
</tr>
<tr>
<td>DDR3</td>
<td>x4, x8,16 socketed, solder down and direct attach interposers</td>
</tr>
<tr>
<td>DDR4</td>
<td>x4, x8,16 socketed, solder down and direct attach interposers</td>
</tr>
<tr>
<td>LPDDR2</td>
<td>BGA and PoP Interposers</td>
</tr>
<tr>
<td>LPDDR3</td>
<td>BGA and PoP Interposers</td>
</tr>
<tr>
<td>LPDDR4</td>
<td>PoP Interposer</td>
</tr>
<tr>
<td>GDDR5</td>
<td>Solder Down and Socketed Interposers</td>
</tr>
</tbody>
</table>

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5 For use with BGA Interposers only.